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Design and Implementation of DDR SDRAM Controller for Embedded Processors

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Abstract - DDR SDRAM (Double Data Rate Synchronous Dynamic Ram) is SDRAM is very cheap and fast memory used in many industrial applications like signal processing, image /video processing, networking with 2n bit high speed data fetch architecture. The SDRAM accesses are easily controlled with the help of DDR SDRAM memory controller which receives the sequence of commands from the user and performs operations on the DDR SDRAM. The memory controller performs READ, WRITE & REFRESH operations and transmits the user data to memory with double data rate as of the main clock frequency. In this paper the memory controller design using Xilinx 14.7 HDL verilog is explained.

Key Words: Synchronous Dynamic RAM (SDRAM), Double Data Rate (DDDR), DDR SDRAM Controller

INTRODUCTION

With the increase in the speed of the processers it is requires very high speed memory accesses. The DDR SDRAM can achieve the double data rate with 2n-bit pre fetch architecture. Every processer in electronic components require memory to store the data variable and addresses for further processes such data and address are stored in RAM (Random Access Memory), the address and data variable are accessed anywhere for the memory. Hence the processer can access the data quickly and faster than ROM. But The RAM looses the data when the power is turned off hence it is called as volatile memory. Usually RAMs are made of MOSFET Transistor cells. Each cell stores single bit of data. Such memory is arranged in to two dimensional grids. Memory cells are etched on to silicon wafer in columns (bit lines) and rows (word lines). The inter connection of the bit line and word line constitutes a memory cell.

There are two types of RAMs Static RAM (SRAM), Dynamic RAM (DRAM). Static RAM: The Static RAM uses a flip-flop to store bits. The RAM is called static because once the processors write the data into bit line it remains unchanged until the processors modify the bit stored in that particular bit line. There are six transistors placed in single cell to store single bit of data information. The SRAM is very fastest memory and data is stored and remained in the memory even though power is off. Dynamic RAM: The dynamic ram is made up of a single transistor and a capacitor. The leaky capacitors store the binary digits in the form of charges. The memory needs to be refreshed periodically because the capacitor looses the charges after write and read accesses hence it is called as dynamic memory. The DRAM is slow compared to SRAM and uses less space to store charges and is inexpensive. Synchronous DRAM: SDRAM is the most dominant form of DRAM. Each cell is organized in rows and columns. In SDRAM the memory is divided into four memory banks followed by row and column address, Whenever the data is to be stored or received from the memory the CAS(column address and RAS (row address select)signals are to be accessed. The SDRAM needs to be refreshed which uses extra circuit to control the refresh operations. There are two different types of SDRAM. The SDR SDRAM which send the data only on the rising edge of the clock and DDR SDRAM which sends and accepts the data on the both edge of the clock to achieve the high speed data transfers. The DDR SDRAM also supports different burst transfer operations. The DDR SDRAM uses the memory controller to achieve the double data rate, The DDR controller uses the commands such as REFRESH, ACTIVATE, PRECHARGE, WRITE, READ and LODE_MODE to control the operations of SDRAM. In this paper the design of DDR SDRAM controller and its operations are explained. The first section contains

introduction, in the second section the DDR SDRAM controller designs are explained and in the third section the controller FSM's are explained. In the final section the simulation results are explained.

DESIGN OF DDR SDRAM CONTROLLER

The DDR SDRAM controller consists of four functional blocks as shown in Fig 1.

1. Controller interface module
2. Command FSM module
3. Address latch
4. Data path module

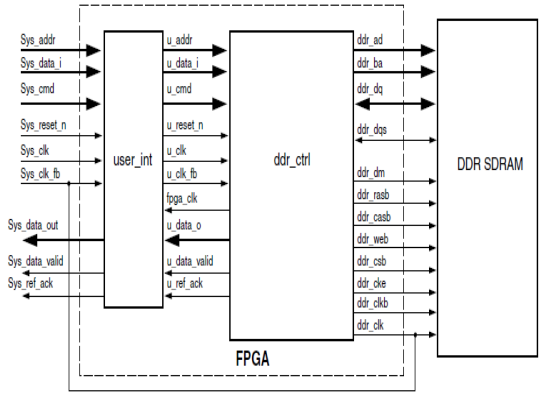

Fig -1: Top level Controller Block Diagram.

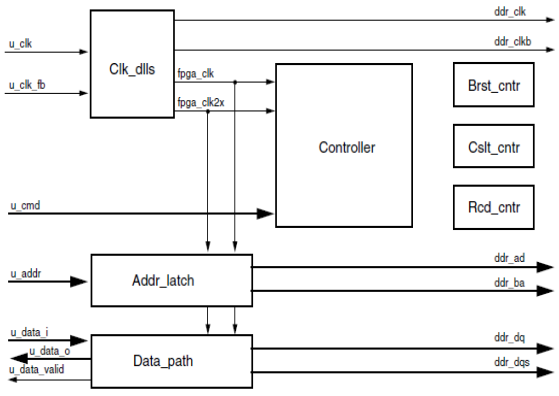

Fig -2: DDR SDRAM Controller Diagram.

2.1. Control Interface module:

This block handles the user information give to the command module it decodes the commands for the command module. This block consists of arbiter to grant the access to the processors and the refresh unit. The block also consists of a refresh unit with registered counter which generates refresh signal periodically.

2.2. Command FSM Module:

This module takes the command from the control interface module and row address, column address, bank information from the address latch. This module generates the required input signals for the DDR SDRAM. This module must be initialized on powered up and then handles the operations required for the DDR SDRAM. The initial module in the command FSM must be initialized in a predefined manner to overcome the undefined operations.

2.3. Data path Module:

This module performs the data latching and data dispatching on data provided by the user or DDR SDRAM. The module takes n-bit of information and generates 2n-bit signal with double data rate. The module handles the data latching operations for bursts lengths.

2.4. Address Latch:

This module holds the address information required for the command module this module receive the user address information and generates the row column address. This module also holds the load mode register address.

DDR SDRAM CONTROLLER FSM COMMANDS

The table 1 given below shows the different commands for DDR SDRAM Controller. The controller receives different commands from user and performs different operations.

Table -1: DDR SDRAM Controller FSM Commands

Function	CS	RAS	CAS	WE
IDLE	L	X	X	X
NO-OPERATION	L	H	H	H
ACTIVE	L	L	H	H
READ	L	H	L	H
WRITE	L	H	L	L
BURST TERMINATE	L	H	H	X
PRECHARGE	L	L	H	L
AUTO-REFRESH	L	L	L	H
LOAD MODE REGISTER	L	L	L	L

3.1. IDLE

In this state the controller remains IDLE, The controller remains in this state until the reset is asserted and the command is initiated.

3.2. NO OPERATION (NOP):

The NOP command is issued to select and enable the DDR RAM. In this state the previously registered commands already in progress are not affected.

3.3. ACTIVE (ACT)

The active command is used to open row from the particular bank. The bank is selected based on the address information provided by the users. Once the active command is issued then read and write operations can be performed.

3.4. READ:

The read operation is issued after the row is selected in the ACTIVE command. During the READ operation the data from the SDRAM is read on DQ signal line of data path module. The sequence of data is transferred from the row address issues in the active command until the burst is over. Once the READ operation is finished the controller will issue the PRECHARGE command.

3.5. WRITE:

The WRITE command is issued by the controller after the ACTIVE command. During WRITE operation the user data to be written on the DDR SDRAM is sent through the data path module with double data rate, once the write operation is done then the controller issues the PRECHARGE command.

3.6. PRECHARGE (PRE)

The pre-charge command is issued after read/write operation. This command deactivates the selected row in the bank. The bank and row addresses are selected during this stage and A10 input bit of the row address is pre-charged.

3.7. BURST TERMINATE (BST)

The memory controller issues this command once the sequential read or write operations are completed. This command is followed by closing the particular bank selected during the write or read operation.

3.8. LOAD MODE REGISTER (LMR)

The load mode register stores data information which defines the operation of the DDR SDRAM, including the burst length, CAS latency, Burst type. The Load mode register bit defines the particular operations as shown in the fig. 3.

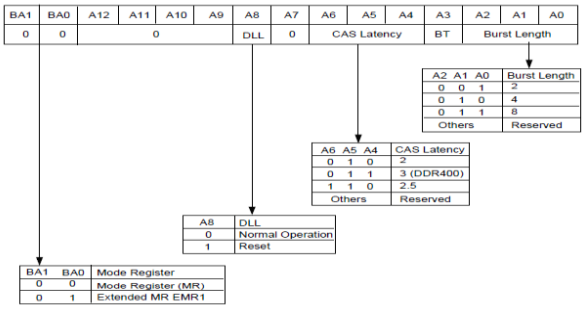

Fig -3: Load Mode Register Blocks

DDR SDRAM CONTROLLER FSM

The DDR SDRAM controller FSM is as shown in the fig. 4.

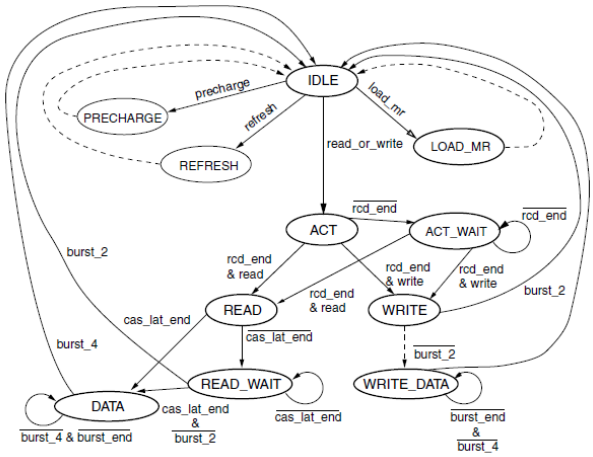

Fig -4: Controller Command FSM.

The Controller command FSM is as shown in the fig 5. The controller remains in IDLE state until the command is issued by the controller. The READ and WRITE operations are issued by the controller once the after particular row address is selected during the ACTIVE state, The controller waits in READ states until the cas latency is finished and then the data ia accessed from the DDR SDRAM, once the burst has finished the controller jumps to IDLE state and then it is PRECHARGED. Similarly the WRITE state is used to write the data into DDR SDRAM after rcd delay is finished during the ACTIVE state. Once the data burst is over the controller goes to IDEAL state. The controller is refreshed periodically during the refresh state. LOAD_MR state is used to load the load mode register which defines the operations of the controller.

SIMULATIONS RESULTS

The DDR SDRAM controller design simulations are done using HDL verilog code in Xilinx 14.7 tools. The synthesis is done using Xilinx ISE tools.

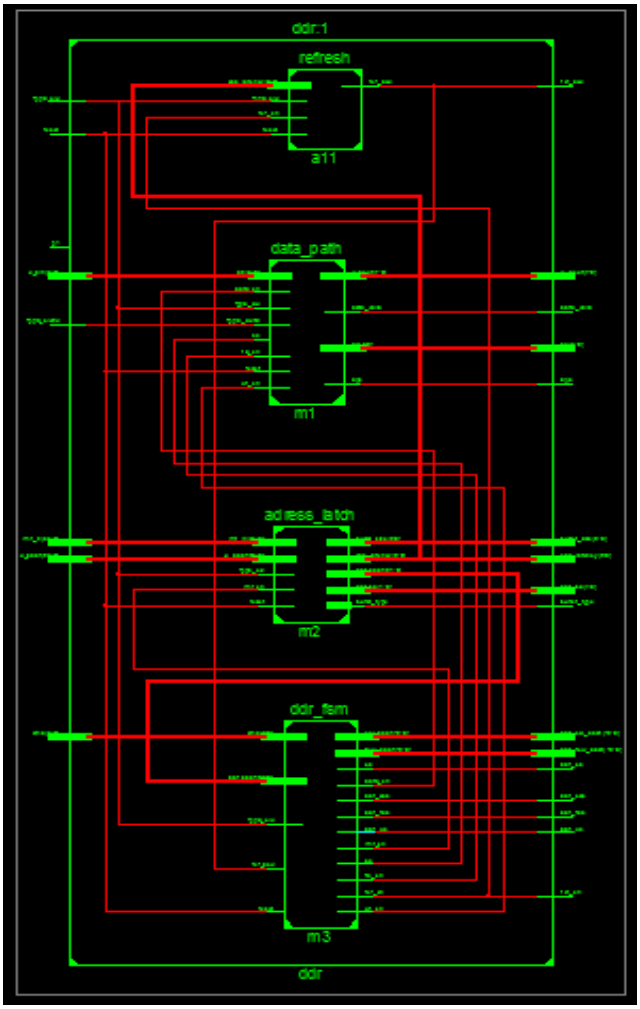

Fig -5: RTL Schematic of DDR SDRAM Controller

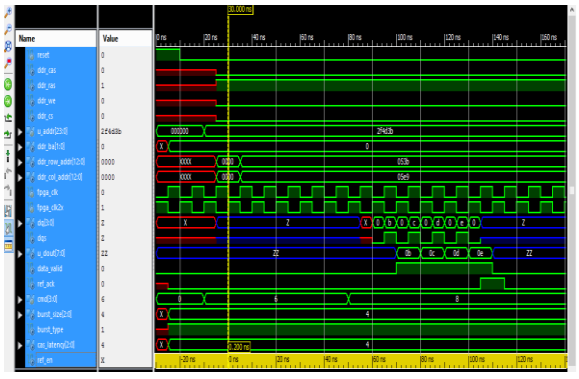

Fig -6: DDR SDRAM READ Operation.

Read Operation

During the Read operation the data is received from the DDR SDRAM on DQS single line with double data rate.

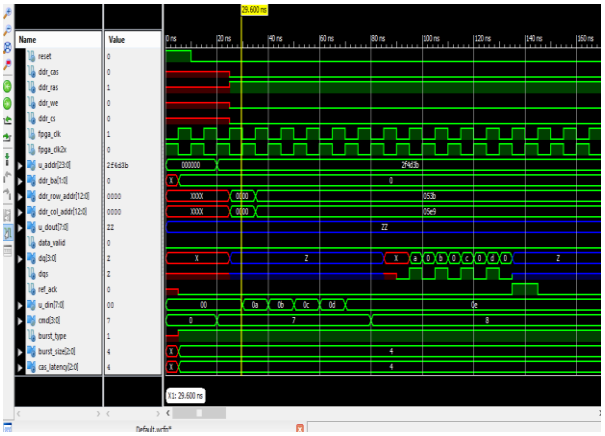

Fig -7: DDR SDRAM WRITE Operation.

Write Operation

During the write operation the data is sent form the users on DQS signal line form the controller with double data rate.

CONCLUSION

In this paper the architecture of High Speed DDR SDRAM controller design with burst transfer is explained. Traditional single data rata (SDR) SDRAMs are limited in their interfaces, therefore the DDR SDRAM are introduced as an enhancement. DDR SDRAM enables high speed data transfer operations by row and column accesses. DDR SDRAM is volatile and complex memory device The controller is used to synchronize the data transfer between the embedded processor and the DDR SDRAM. This controller can be used to achieve double data rate data transfer between the memory and the processors. The controller synchronizes the burst oriented data transfer. In this paper an efficient design of DDR SDRAM is explained and the simulations and synthesis reports are generated for different cases using Xilinx 14.7 tools.

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